
Impact of Thermal Analysis on Large Chip Design

Dr. Rajit Chandra

Electronic Design Process Symposium

Monterey, CA

April 7, 2005

Outline

- Why thermal analysis?
- Thermal impact on silicon performance
 - Cell and interconnect delay
 - Leakage power
 - Mean time to failure
- Thermal analysis method
 - 3D thermal model for IC and its environment
 - On-chip analysis tradeoffs for accuracy versus speed
 - Pre-layout and post-layout thermal analysis
- Thermal analysis flow integration
 - Power analysis
 - Timing analysis
 - Extraction
 - Delay calculation
 - Rail analysis
 - Voltage drop
 - Electromigration
- Conclusion

Why thermal analysis?

Heat forces Intel to cancel desktop chips:

LONDON -- Intel Corp. plans to announce Friday (May 7) that it has cancelled its next chips for desktop and server computers, codenamed Tejas and Jayhawk, The move represents a significant shift in Intel's development plans and a desire to build chips that are computationally powerful without generating excessive amounts of heat,

Move to large scale integration by Texas Instruments:

Monday, January 24, 2005 4:28 PM Subject: Texas Instruments (TXN) today announced Nokia will incorporate a single-chip solution based on TXN's Digital RF Processor (DRP) technology into its future phones. ... TXN now has the technology to integrate digital baseband, SRAM, logic, RF, power management and analog functions into a single 90nm CMOS chip Another criterion for 90-nm process technology is power consumption. Portable devices operate on batteries, so minimizing power consumption is key But there are limits to the heat that an IC can reasonably dissipate, which leads to device leakage and power dissipation.

International Technology Roadmap for Semiconductors:

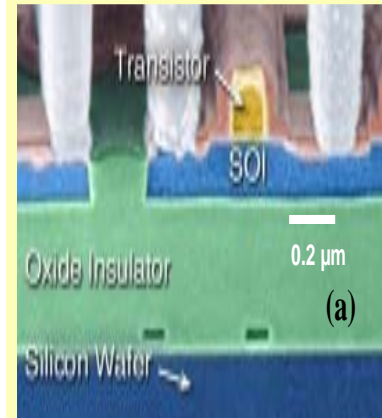
A knowledge deficit in heat and an absence of thermal tools will force leading chip designers to apply costly timing and power margins at 10%-15% today to 30%-40% in 3 years.

Temperature makes or breaks silicon

- Self heating and thermally induced electrical effects are pressing issues for nanometer scale semiconductors
- Absolute temperature and temperature gradients impact:
 - Timing
 - Power
 - Reliability
- Understanding the challenges and the available thermal technology is key to finding the solutions

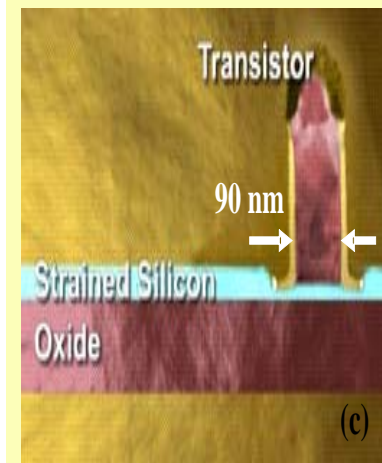
Silicon-On-Insulator (SOI)

IBM 2001



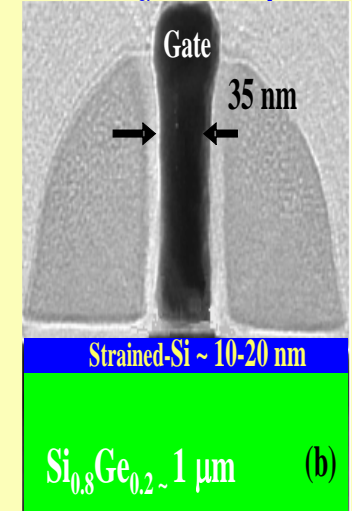
SS Directly-on-insulator (SSDOI)

IBM-IEDM, Washington DC, Dec 7, 2003

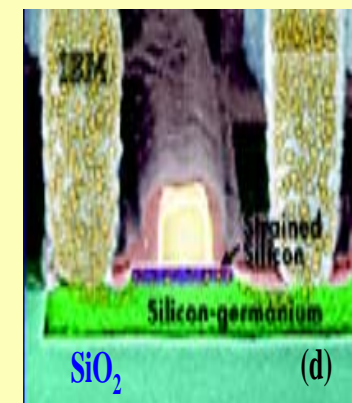


Strained-Si (SS) NMOS

AMD, Technology Research Group



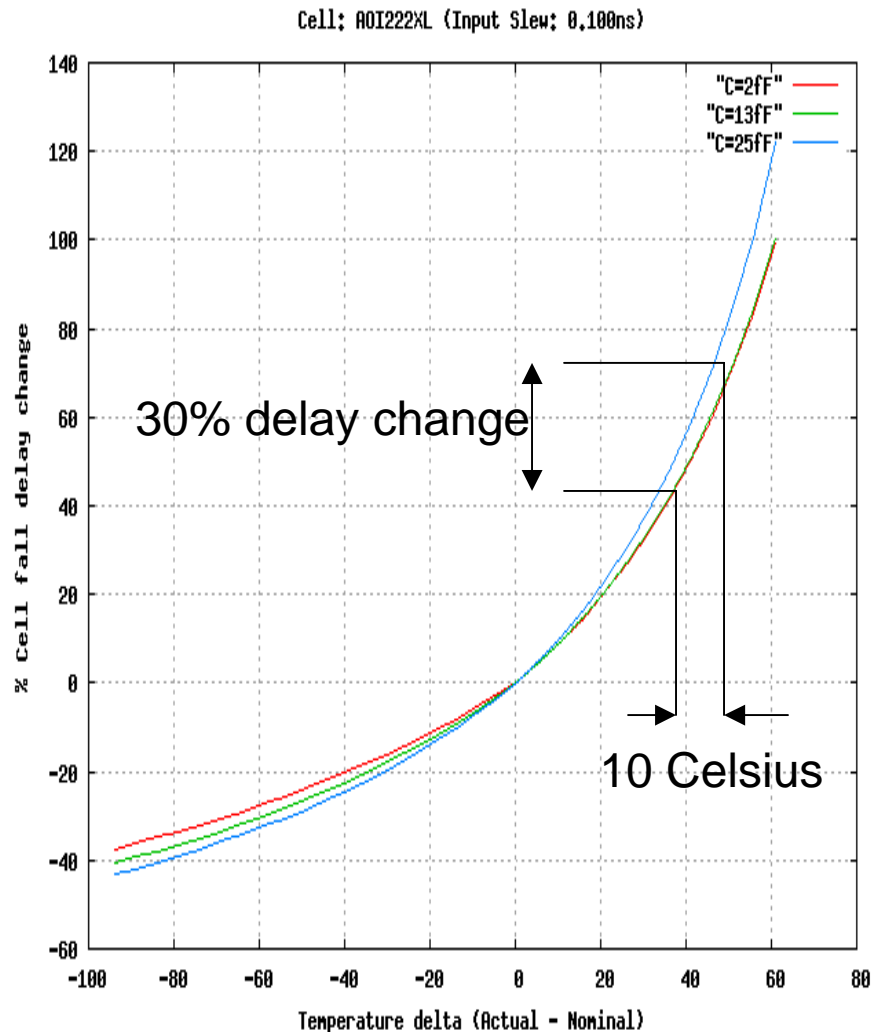
Strained-Si on Silicon dioxide



Thermal impact on Silicon Performance

- Cell and interconnect delay
- Crosstalk noise and delay
- Leakage power
- Mean time to failure

Cell delay



- Cell delays and signal slew vary due to temperature affecting drive strength – as the most dominant effect
- Effective load changes due to change in wire resistances
- ***Delay varies up to 30% for temperature variation of 10° C***

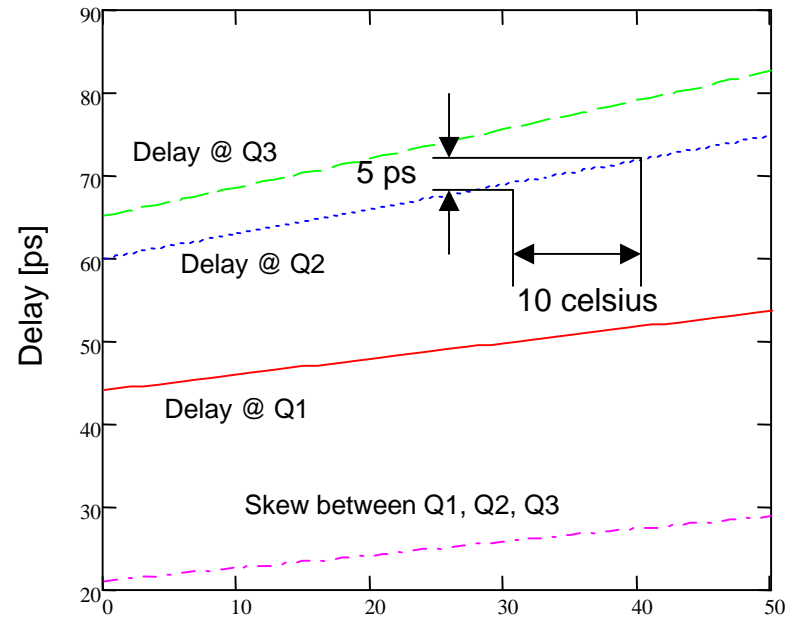
Interconnect delay



Hot region

Cold region

- Example: 1mm wire with driver in hot region, receivers in cool region
- Temperature difference of 10°C results in 5 ps ($\sim 8\%$) delay difference

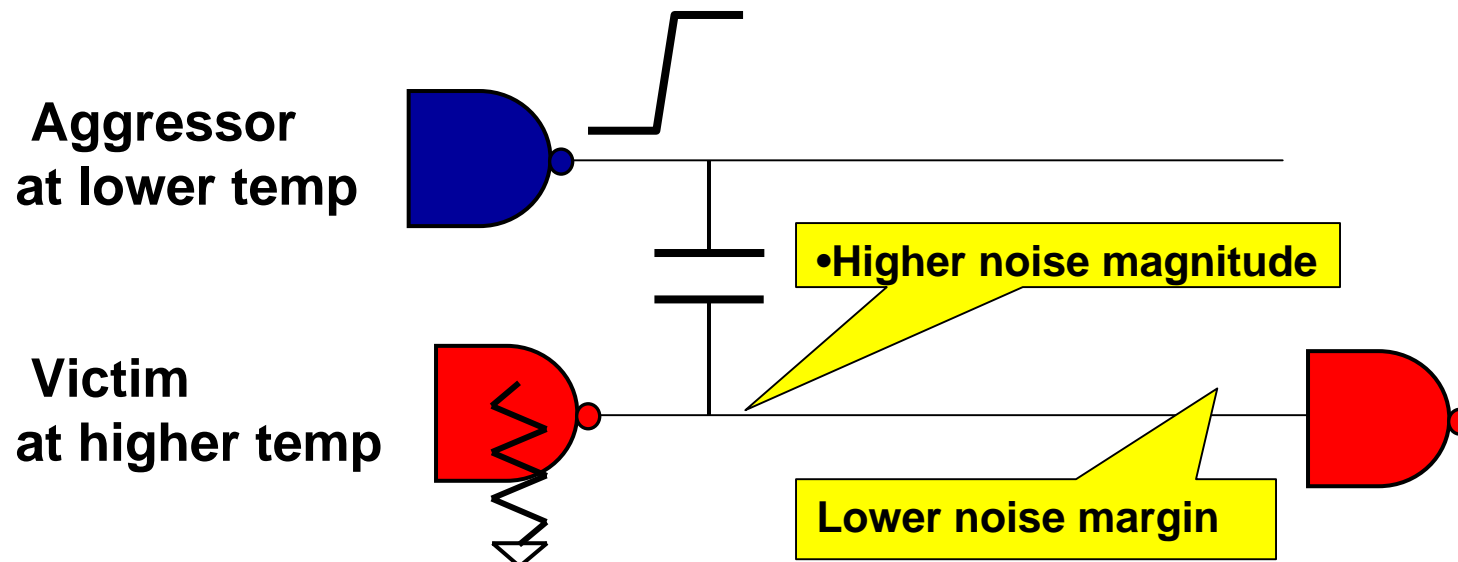


Temperature difference between cold and hot region [Celsius]

Crosstalk noise

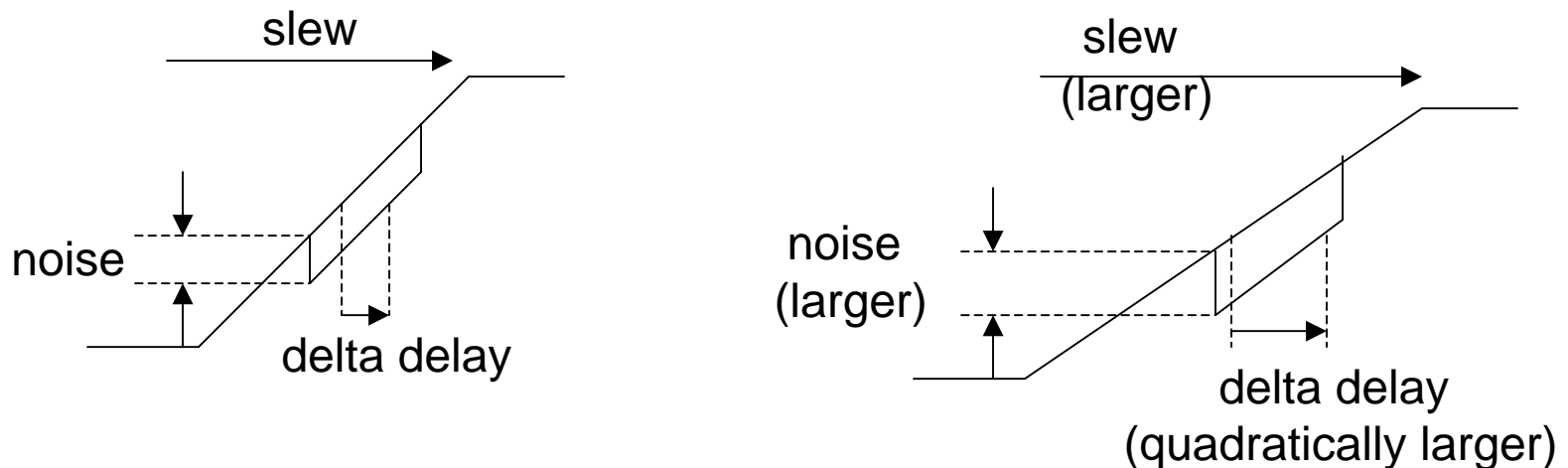
Effect of temperature increase of 10°C on

- **Noise magnitude**
 - 20% increase of driver resistance R_d
 - 5% increase of wire resistance R_w
 - 25% increase of noise magnitude, if $R_d = R_w$
- **Noise margin**
 - 2.5% decrease in threshold voltage
 - 2.5% percent decrease in noise margin
 - Directly proportional to noise magnitude increase



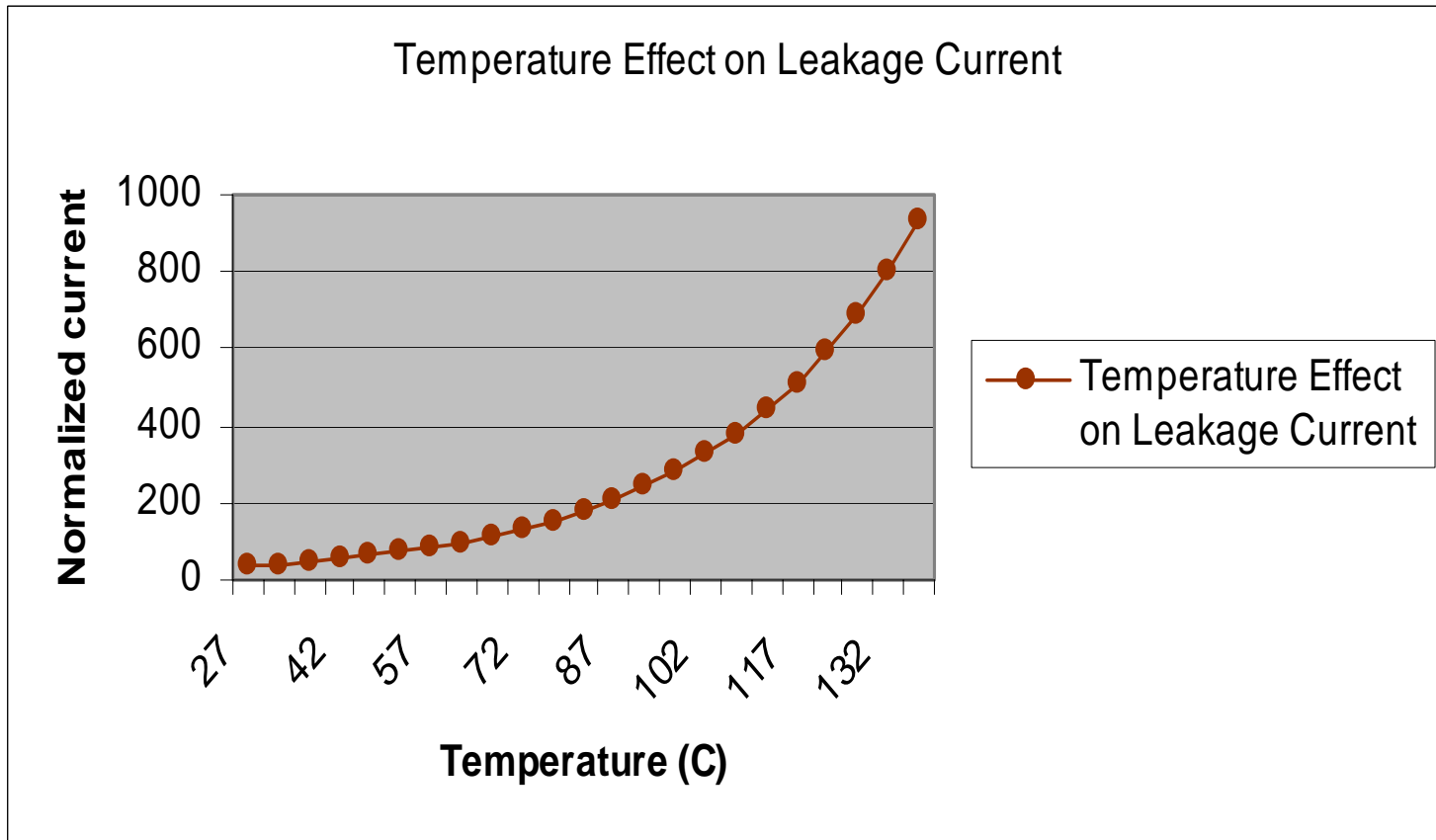
Crosstalk delay

- Larger victim driver resistance leads to slew degradation and delta delay increase
- Larger noise magnitude superimposed with larger slew leads to proportionally larger delay increase
 - noise * 125%
 - slew * 125%
 - delta delay * (125%)² = delta delay * 156%



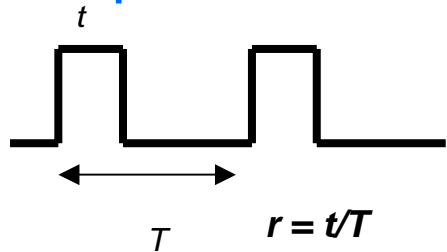
Leakage power

- Leakage current and hence leakage power increase exponentially with temperature



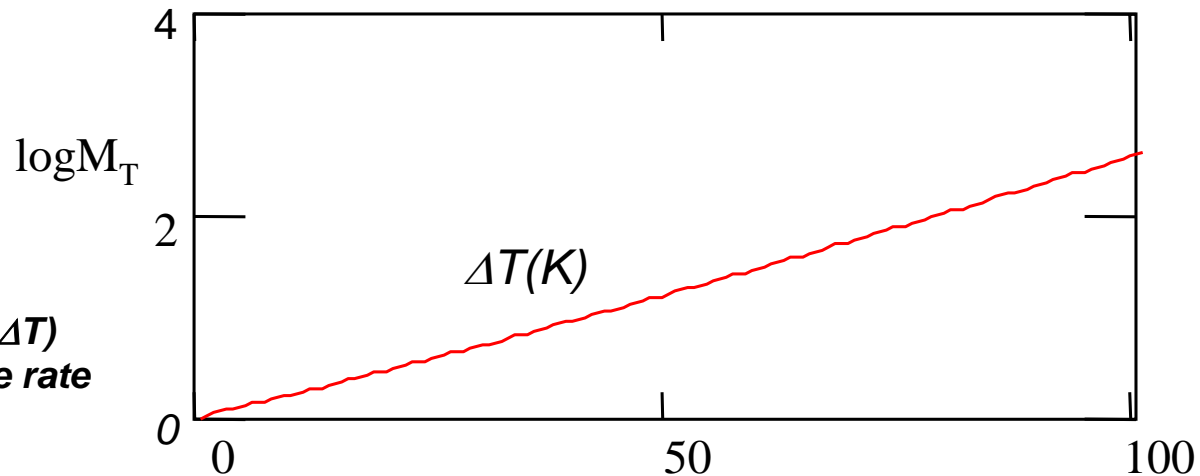
Mean time between failure (MTBF)

- Self heating in power grid reduces MTBF
- Thermal migration of metal ions encourages electromigration
- Exponential life time reduction due to temperature



$$MTBF = A \cdot J_{avg}^{-2} \cdot e^{\left(\frac{Q}{k \cdot (T_{ref} + \Delta T(J_{rms}))}\right)}$$

$M_T = \text{normalized value of } MTBF(300K)/MTBF(300K + \Delta T)$
 Provides measure of failure rate



Summary so far

- Even a temperature gradient of 10°C has significant impact on
 - Delay: up to 30%
 - Noise: up to 25 %
 - Leakage power: exponential increase with temperature
 - Life time: exponential decrease with temperature
- Thermal analysis is needed

Thermal analysis method

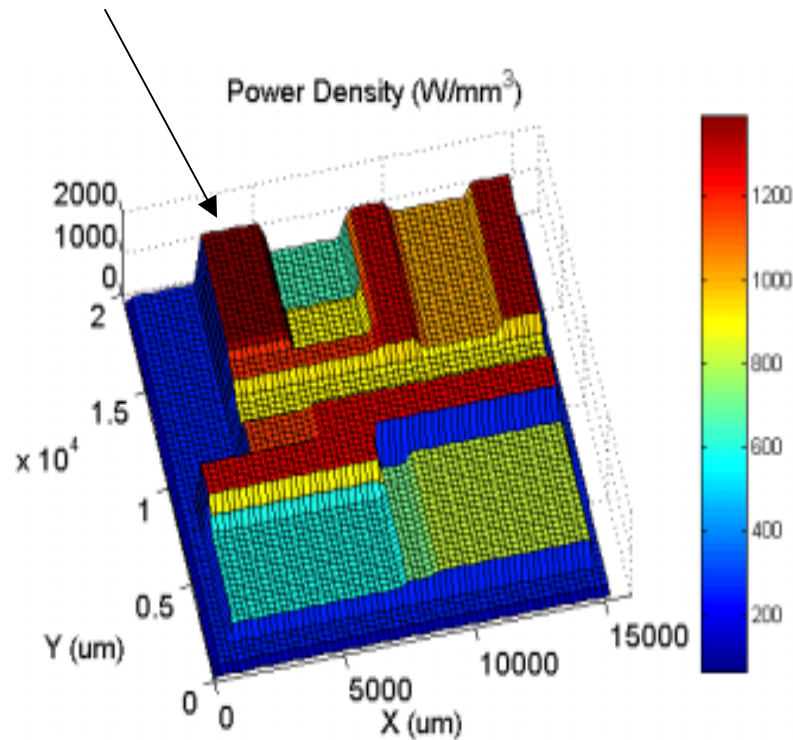
- 3D thermal model for IC and its environment
 - Temperature estimates across full chip accounting for
 - Silicon material, dimensions, package parameters, cooling systems, ambient conditions
- On-chip analysis tradeoffs for accuracy vs. speed
- Pre-layout and post-layout thermal analysis

Problem statement

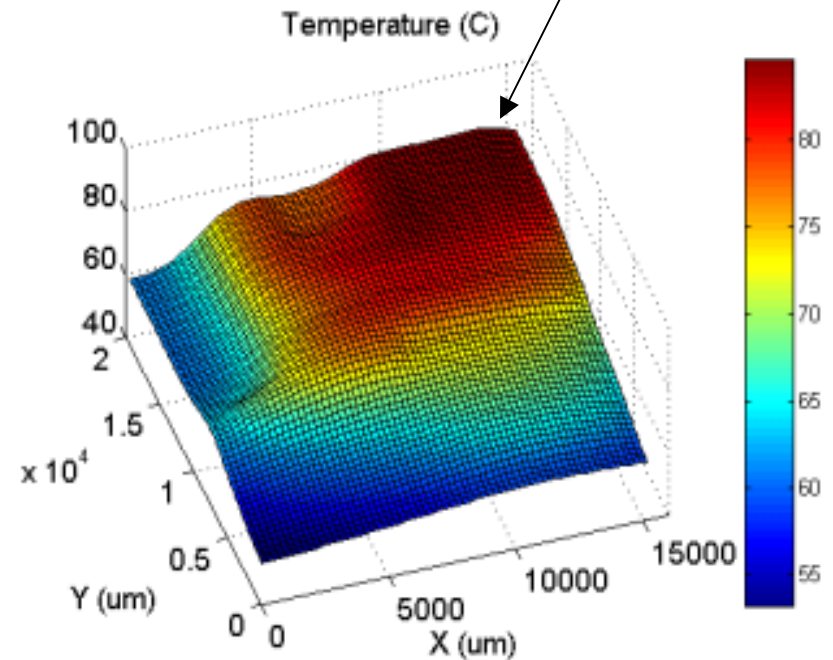
- Chip temperature is not constant
 - Large chips, varying power densities
 - Breaks the fundamental premise of design analysis and implementation
- Requires full-chip temperature calculation
- Capability to retrofit the existing tools with the impact of 3D on-chip temperature variations to account for changing characteristics of the design

Power density versus temperature

Location with highest power density



Location with highest temperature

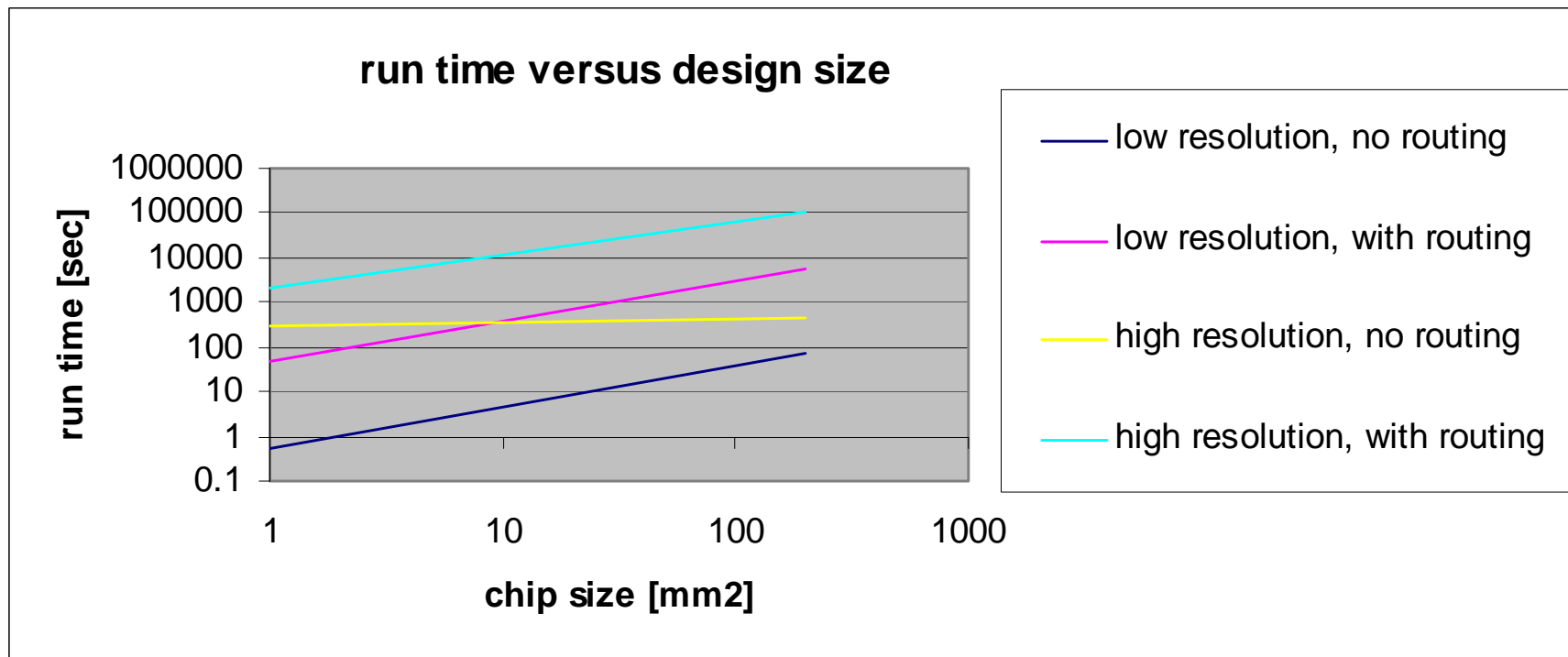


Power and temperature distribution are different

Source: ICCAD 2004

Thermal analysis runtime vs. design size

- Low resolution: several physical objects are lumped together as a volume with constant temperature
- High resolution: every physical object is treated as separate volume
- No routing: Metal layers modeled as homogeneous medium with constant thermal conductivity
- With routing: Thermal conductivity of each routing segment is taken into account



Accuracy vs. analysis mode

Design 1

Avg. temperature = 65°C

Analysis mode	Highest temperature gradient [Celsius]
Low resolution, no routing	4.1
Low resolution, with routing	3.9
High resolution, no routing	10.3
High resolution, with routing	8.3

Design 2

Avg. temperature = 75°C

Analysis mode	Highest temperature gradient [Celsius]
Low resolution, no routing	12.0
Low resolution, with routing	11.9
High resolution, no routing	10.3
High resolution, with routing	10.2

Pre-layout thermal analysis

- Estimate the power consumption of major blocks
- Do the floorplan
- Calculate the temperature distribution for the floorplan
 - Low resolution, without routing
- Do floorplan changes for global temperature equalization
- Do detailed placement
- Calculate the temperature distribution for detailed placement
 - High resolution, without routing
- Do placement changes for local temperature equalization

Post-layout thermal analysis

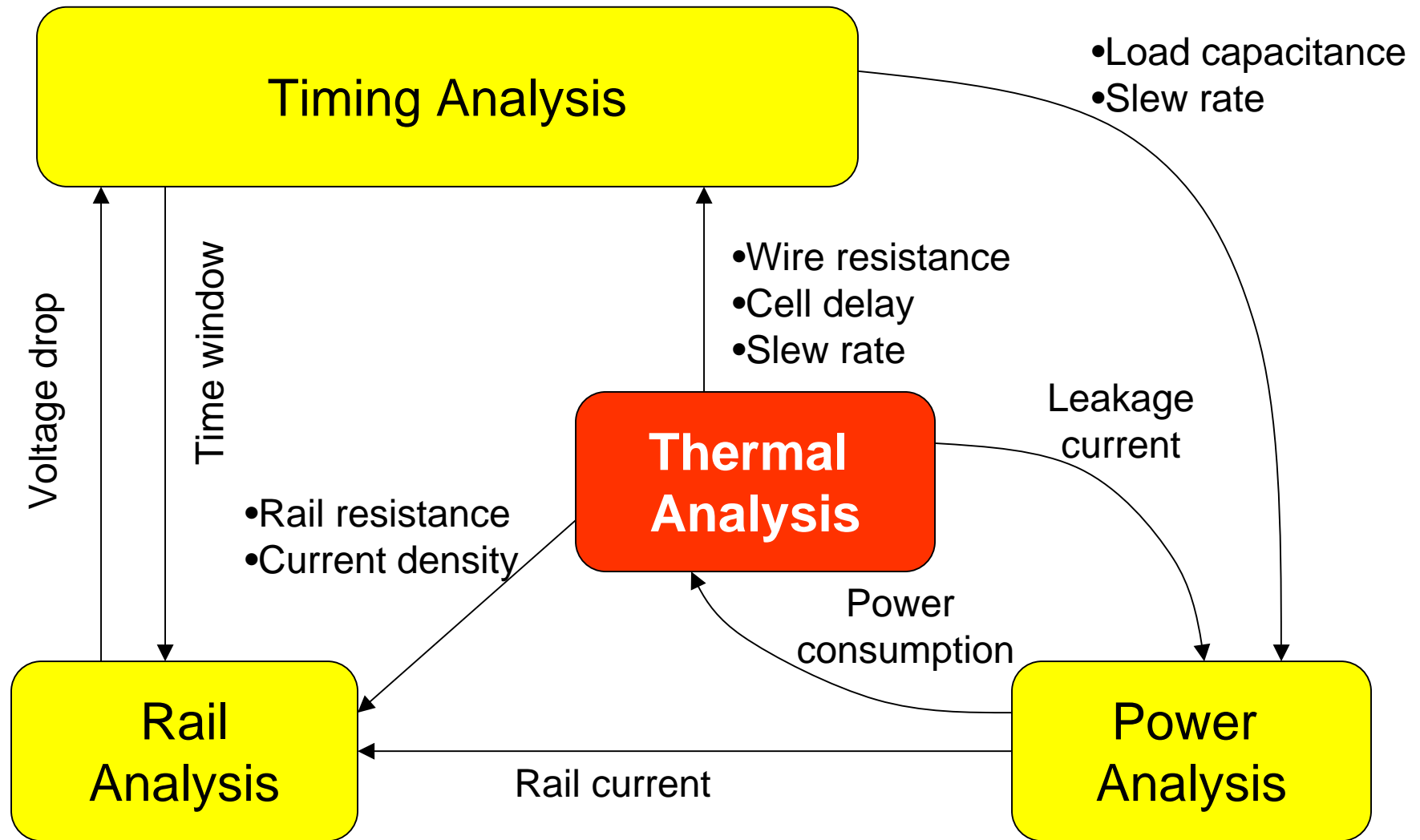
- Calculate the temperature distribution
 - Low resolution, with routing
- Calculate stable operation condition for power consumption and temperature
- Annotate temperature effect to the extracted parasitics
- Calculate temperature impact on timing, crosstalk, voltage drop, and electromigration
- Apply ECO and repair actions to lower temperature gradients
- Calculate the temperature distribution for final sign off
 - High resolution, with routing

Thermal analysis flow integration

Solving the interdependency between thermal analysis and

- Timing analysis
 - Extraction
 - Delay calculation
- Power analysis
 - Dynamic
 - Static
- Rail analysis
 - Voltage drop
 - Electromigration

Thermal analysis affects everything



Temperature-aware timing analysis

Extraction

- Calculate parasitics under average temperature condition
- Scale wire resistance according to temperature gradient

Delay calculation

- Calculate delay, slew, time windows under average temperature condition
- Scale delay and slew according to temperature gradient
- Shift time windows according to temperature gradient

Temperature-aware power analysis

Dynamic power

- Use the temperature-adjusted slew for power calculation
- Use the temperature-adjusted time windows for instantaneous current calculation

Static power

- Calculate leakage power as a function of temperature
- Recalculate temperature as a function of leakage power
- Find the stable operating point

Temperature-aware rail analysis

Extraction

- Scale the power rail resistance according to temperature

Voltage drop

- Use the temperature-adjusted power and rail resistance data to calculate rail currents
- Use the temperature-adjusted timing data to calculate instantaneous voltage drop

Electromigration

- Check the rail current density against temperature-dependent current density limits

Conclusion

- Thermal analysis is needed
- Thermal analysis for large designs is feasible
- Thermal analysis needs to interact with other analyses
- Thermal analysis can drive physical design optimization